AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-35 (Canceled)

36. (Currently Amended) An array substrate for use in a transflective liquid crystal display device, comprising:

a transparent substrate;

at least one gate line and at least one gate electrode formed on the transparent substrate;

a gate-insulating layer formed over the at least one gate line and the at least one gate electrode;

a silicon layer formed on the gate-insulating layer, the silicon layer being positioned above the at least one gate electrode;

a source electrode and a drain electrode formed on the silicon layer and spaced apart from each other with the silicon layer overlapped therebetween, wherein the at least one gate electrode, the source electrode, the drain electrode, and the silicon layer define a thin film transistor (TFT);

at least one data line;

a first passivation layer covering the at least one data line;

a transparent electrode formed on the first passivation layer; and

a reflective electrode formed on the transparent electrode, the reflective electrode having a double-layered structure.

37. (Canceled)

38. (Previously Presented) The arrays substrate of claim 36, further comprising a second passivation layer between the transparent electrode and the reflective electrode.

39. (Currently Amended) The array substrate of claim 36~~37~~, wherein a first reflective electrode layer is a corrosion-resistant metal layer.

40. (Previously Presented) The array substrate of claim 39, wherein the corrosion-resistant metal layer is one of chromium and molybdenum.

41. (Currently Amended) The array substrate of claim 36~~37~~, wherein a second reflective electrode layer is an aluminum-based layer.

42. (Previously Presented) The array substrate of claim 39, wherein the aluminum-based layer is one of aluminum and aluminum neodymium.

43. (Previously Presented) The array substrate of claim 36, wherein the gate line and gate electrode have a double layered structure.

44. (Previously Presented) The array substrate of claim 43, wherein a first gate line and gate electrode layer is one of aluminum and aluminum neodymium.

45. (Previously Presented) The array substrate of claim 43, wherein a second gate line and gate electrode layer is titanium.

46. (Previously Presented) The array substrate of claim 36, wherein the first passivation layer is one of benzocyclobutene, acryl-based resin, and silicon oxide.

47. (Previously Presented) The array substrate of claim 45, wherein the first passivation layer is silicon oxide and the second passivation layer is silicon nitride.

48. (Previously Presented) The array substrate of claim 45, wherein the transparent electrode is one of indium tin oxide and indium zinc oxide.